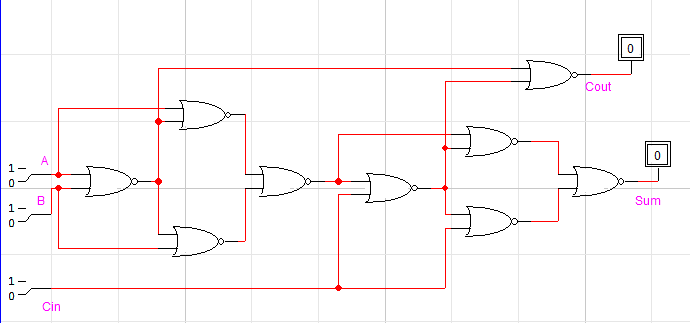
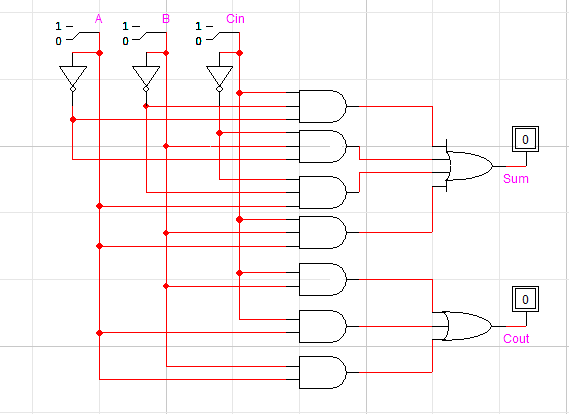
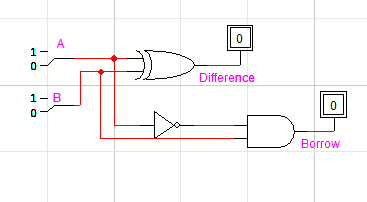
**DLD Assignment**

Q7) Design Full Adder Circuit using only NOR gates only Circuit in Logic Works.

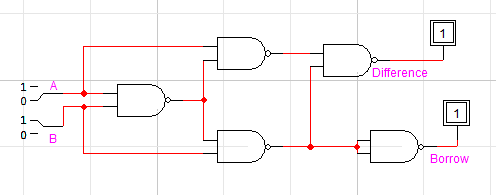


Q8) Design Full Adder Circuit using primary gates only Circuit in Logic Works.

Q9) Design Half Subtractor Circuit in Logic Works.



Q10) Design Half Subtractor Circuit using only NAND gates only Circuit in Logic Works.



Q11) Design Half Subtractor Circuit using only NOR gates only Circuit in Logic Works.

